M.Tech (CSE) 3rd Sem-2019

Sub: Distributed Systems

Time: 3 Hours **Full Mark: 70**

(Answer all questions and the figures in the right hand margin indicates marks)

Q1. a) Compare among Distributed systems, Network Systems and Parallel systems considering the necessary properties. [7]

b) Differentiate between Loosely Coupled and Tightly Coupled Systems. Hence, compare the properties of Multi-Processor and Multi-Computers. [7]

OR

a) What are Distributed systems? Write in detail the different issues in Distributed computing system. [7]

b) What are the different physical forms of Interconnection Networks are available. Compare between Multi Port Memory and Cross Bar Switch Network. [7]

Q2. a) What are the different components available in a PE. Explain the functions of each component. [7]

b) Explain how the data routing function works in an Array Processor for the following with N=8. Write the total number of steps required for performing this operation. [7]

$S(K)=\sum_{i=0}^{k} A_i$ for k=0, 1, 2…n-1

OR

a) What are the various Network Design Decisions for Inter PE communication based on? Explain each of them with types. [7]

b) Compare between [7]

i) Single Stage and Multi Stage Interconnection Network

ii) Static and Dynamic Interconnection Networks

Q3. a) Design a mesh connected ILLIAC IV network with N=16. Write the routing function and the upper bound on routing steps.

Find the steps required so that PE7 can communicate with PE13. [7]

b) Design a Shuffle Exchange interconnection network for N=16. Write perfect shuffle, inverse perfect shuffle and apply the exchange function on both. [7]

OR

a) Explain the design of cube interconnection network. Find the data routing functions of Cube Interconnection Network. How the multi stage permutation is conducted in an n-stage Cube Network. [7]

b) Draw and find the data routing functions of PM2I interconnection networks of N=16. Write the routing function and the upper bound on routing steps.

Find the steps required so that PE7 can communicate with PE13. [7]

Q4. a) Explain with diagram how the matrix multiplication takes place for a 3 X 3 matrix in an ILLAC-IV involving all 64 PEs in synchronous lock-step fashion. Consider the case for Problem size N=64, N>64 and N<64. [7]

b) Draw the BSP System Architecture and Explain the operation through its components. [7]

OR

a) Consider a BSP System consists of 7 memory modules and 6 arithmetic elements. Show the physical memory mapping of a 4 X 5 matrix in that BSP system. Hence, Compute the compute the module and offset for the second row of the array. [7]

b) Write the $O(N^2)$ algorithm for SIMD Matrix multiplication and explain the step of operation through a diagram. [7]

Q5. a) Draw the data flow graph for the computation of

$$U = f(x, y) = ((x * y)\frac{x*y}{y}x - \left(\frac{x*y}{y}\right) + (y * x) - x * (\frac{x*y}{y})) \quad [7]$$

b) Explain different parameters used for evaluating the static interconnection networks. Give a comparison table of characteristics considering the following static interconnection networks. [7]

OR

a) Derive the equation for performance analysis of Array Processors. Compute the Total time required to execute the job, Time required to execute i^{th} instruction, its speedup and efficiency. [7]

b) What is PRAM? Explain the subclasses of PRAM [7]