III–S-(5 Yr.)–IMCA–II-(CA)

(2019)

Full Marks – 70 **Times: 3hr**

The figure in the right hand margin indicates marks.

(Answer all Questions)

Q.1 a) Differentiate between logical cache and physical cache . Which type of cache is a better option and why ? [6

b) What is cache mapping. Which type of mapping is the best implemented and why? Given the following data, use 4-way Set-Associative mapping to perform mapping and find the set number and line no. Main memory address generated by the CPU is 00000100011

Main memory capacity =64 blocks
Block size= 16 words
Word length=16bits
Cache size= 32 lines

[8

OR

c) Explain the Hamming code Algorithm for detecting and correcting errors. Take your own error example to detect the location of error [6

d) Discuss the characteristic of cache memory in ARM organization. [4

e) Write notes: [4

-> Write-back policy

-> SDRAM

Q.2 a) Discuss the features of RAID devices. Where are they used? Write the merits and demerits of the first 2 RAID levels. [7

b) Differentiate between programmed IO and interrupt driven IO. Explain the interrupt handling method in which a program is used to check interrupt by the Processor.

[7

OR

c) What steps a processor takes, when a interrupt occurs. [4

d) State the method of data redundancy in RAID level 3. [4

e) Which type of memory are the fastest. Discuss the method used for performing IO between main memory and secondary storage. [6

e) Write notes . [4

->Thunderbolt

-> IO module

Q.3

a) State the instruction types supported in Intel x86 architecture. Write some basic differences between an Intel x86 and ARM instruction. [10

b) What are the elements of an Assembly language instruction? [4

OR

c) Discuss the memory organization in x86 architecture. What registers are used in finding the effective address of operands. State their use. [10

d) State the addressing modes in ARM. [4

Q.4 a) What is pipelining ?How it is different from serial and parallel processing ? [7

b) Sate the structure of a processor? Discuss the register types in a processor. [7

OR

c) Discuss the following. [6

- ➔ Instruction Cycle
- ➔ Instruction level parallelism

d) State the characteristics of x86 processor. [8

Q.5 a) State the types of multi-processor organization based on memory usage. Give examples [10

b) Discuss multicore organization. [4

OR

c) What is cache coherence ? Discuss its solution. [8

d) Write notes [6

-> NUMA

->Clusters